



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:) Group Art Unit: 2811
Shunpei YAMAZAKI et al.) Examiner: S. Hu
Serial No. 09/334,646) CERTIFICATE OF MAILING
Filed: June 17, 1999) I hereby certify that this correspondence is being
For: SEMICONDUCTOR DEVICE AND) deposited with the United States Postal Service with
FABRICATION METHOD) sufficient postage as First Class Mail in an envelope
THEREOF) addressed to: Commissioner for Patents, P.O. Box 1450,
) Alexandria, VA 22313-1450, on: 1-13-04
) Adrian Stamps

REQUEST BY APPLICANT FOR INTERFERENCE WITH PATENT

UNDER 37 CFR § 1.607

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The Applicants seek to have an interference declared between the above-referenced application and U.S. Patent No. 6,355,940 to Koga et al.

The present application Serial No. 09/334,646, was filed June 17, 1999, and is a Division of Serial No. 08/938,310, filed September 26, 1997, now U.S. Patent No. 5,959,313, which itself is a Division of Serial No. 08/513,090, filed August 9, 1995, now U.S. Patent No. 5,731,613, all of which claim foreign priority under 35 U.S.C. § 119 to JP 6-218077, dated August 19, 1994. Therefore, the effective U.S. filing date of the present application is August 9, 1995, and the earliest effective filing date of the present application is August 19, 1994.

In accordance with 37 CFR § 1.607(a)(1), the Applicants hereby identify U.S. Patent No. 6,355,940 to Koga et al. The '940 patent issued on March 12, 2002, and resulted from application Serial No. 09/148,854, which was filed on September 4, 1998. The '854 application includes a claim of priority under 35 U.S.C. § 119 to JP 9-243057, filed September 8, 1997. It is noted that the claim of priority was not perfected during prosecution of the '854 application.

Since the present application has an earlier effective filing date than the '940 patent, the Applicants respectfully request that they be designated the senior party in a declaration of the interference.

In accordance with 37 CFR §§ 1.607(a)(2) and (3), the Applicants present the following proposed count 1, wherein claim 1 of the '940 patent corresponds exactly to count 1.

1. A display device, comprising:

a plurality of pixel electrodes formed on a substrate;

a plurality of first thin film transistors, which are connected to corresponding pixel electrodes among the plurality of pixel electrodes and respectively supply the connected corresponding pixel electrode with a display signal; and

a plurality of second thin film transistors, which configure a driving circuit for driving the plurality of first thin film transistors; wherein,

some or all of the plurality of second thin film transistors each has a plurality of channel areas formed in a semiconductor layer subjected to laser annealing respectively, and the plurality of channel areas of each respective second thin film transistor are electrically connected in parallel to each other and arranged separately.

Also, claim 5 of the '940 patent corresponds to count 1. Claim 5 is identical to count 1 except claim 5 recites "arranged on a substrate" instead of "formed on a substrate" and "the plurality of channel areas of each respective second thin film transistor are electrically connected to each other and arranged toward different directions" instead of "the plurality of channel areas of each respective second thin film transistor are electrically connected in parallel to each other and arranged separately" (emphasis added). Therefore, the Applicants respectfully submit that claim 5 corresponds to count 1.

In accordance with 37 CFR § 1.607(a)(4), the Applicants identify at least one claim already pending in the present application that corresponds to the proposed count, and explain why each such claim corresponds to the proposed count. Claims 104, 107, 110, 113, 116 and 119 of the present application correspond to count 1. Claim 104 is identical to count 1 except claim 104 does not recite "some or all of." Therefore, claim 104 is

narrower than count 1 and corresponds to count 1. Claim 107 is identical to count 1 except claim 107 recites "some of" instead of "some or all of." Therefore, claim 104 is narrower than count 1 and corresponds to count 1. Claim 110 is identical to count 1 except claim 110 recites "at least one of" instead of "some or all of." The phrase "at least one of" reads on "some or all of." Therefore, claim 110 corresponds to count 1. Claims 113, 116 and 119 are identical to claims 104, 107 and 110, except that they recite "over a substrate" instead of "on a substrate." Therefore, the Applicants respectfully submit that claims 104, 107, 110, 113, 116 and 119 correspond to count 1.

It is specifically noted that claims 1-3, 8, 11-14, 16-19, 32-34, 38-43, 52, 53, 58-60, 65, 71-73, 75-81 and 100-103 are directed to a separately patentable invention and it is respectfully submitted that these claims do not correspond to count 1. As noted in the *Appeal Brief* filed concurrently herewith, independent claims 104, 107, 110, 113, 116 and 119 recite the following features which are not taught or suggested in independent claims 1-3 and 8: (some of or at least one of) a plurality of second thin film transistors each has a plurality of channel areas formed in a semiconductor layer subjected to laser annealing respectively. Also, independent claims 1-3 and 8 recite the following features which are not taught or suggested in claims 104-121: a common gate wiring connected with the at least two transistors at gate electrodes of the at least two transistors; a common source wiring connected with the at least two transistors at one of a source and a drain of each of the at least two transistors; a common drain wiring connected with the at least two transistors at the other of the source and drain of each of the at least two transistors; where the at least two transistors are connected with each other in parallel by the connections of the common gate wiring, the common source wiring, and the common drain wiring with the at least two transistors. Also, independent claims 1 and 3 recite the following features which are not taught or suggested in claims 104-121: a driver circuit including at least one buffer circuit; at least two transistors in the at least one buffer circuit. Therefore, the Appellants respectfully submit that claims 1-3, 8, 11-14, 16-19, 32-34, 38-43, 52, 53, 58-60, 65, 71-73, 75-81 and 100-103 are patentably distinct from claims 104-121.

In accordance with 37 CFR § 1.607(a)(5), the Applicants apply the terms of the application claims identified as corresponding to the count and not previously in the application disclosure to the disclosure of the application. Claims 104, 107, 110, 113, 116 and 119 were added in an *Amendment* filed November 26, 2002. Claims 104, 107, 110, 113, 116 and 119 are supported in the specification of the present invention as follows: a display device (e.g. Fig. 6, see also page 1, line 12) comprising a plurality of pixel electrodes (e.g. page 22, ¶2) formed on or over a substrate (e.g. substrate 15, page 22, ¶2, see also Fig. 6); a plurality of first thin film transistors (e.g. TFT 11, page 22, ¶2), which are connected to corresponding pixel electrodes among the plurality of pixel electrodes and respectively supply the connected corresponding pixel electrode with a display signal (e.g. Embodiment 4, pages 22-23, see also Fig. 6); and a plurality of second thin film transistors (e.g. upper, middle and lower transistors in Fig. 3, see also page 21, ¶3), which configure a driving circuit (e.g. X decoder/driver, Y decoder/driver) for driving the plurality of first thin film transistors (see also page 2, lines 21-22); where (some of or at least one of) the plurality of second thin film transistors each has a plurality of channel areas (e.g. channel-forming region 112, the top of page 16 to the top of page 17, page 20, ¶1 to page 21, ¶2) formed in a semiconductor layer subjected to laser annealing respectively (e.g. page 16, ¶1, see also Figs. 1A and 3, and page 21, ¶2), and the plurality of channel areas of each respective second thin film transistor are electrically connected in parallel (e.g. Fig. 3, top of page 11 to top of page 13; and bottom of page 19 to bottom of page 21) to each other and arranged separately (e.g. Fig. 3).

In accordance with 37 CFR § 1.607(a)(5), the Applicants respectfully submit that the requirements of 35 U.S.C. § 135(b) are met. Claims 104, 107, 110, 113, 116 and 119 were added in an *Amendment* filed November 26, 2002, which is less than one year after the issue of the '940 patent (March 12, 2002). The '854 application leading to the '940 patent was not published. Therefore, the requirements of 35 U.S.C. § 135(b) are met.

In accordance with 37 CFR § 1.607(c), the Applicants identify the following claims in the present application which correspond exactly or substantially to the claims of the '940 patent. As noted above, independent claims 104, 107, 110, 113, 116 and 119 corresponds to count 1, and count 1 is identical to claim 1 of the '940 patent. Dependent

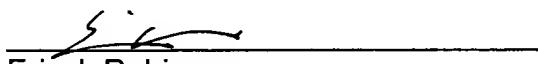
claims 105, 108, 111, 114, 117 and 120 of the present application are identical to dependent claim 2 of the '940 patent. Dependent claims 106, 109, 112, 115, 118 and 121 are substantially the same as dependent claim 4 of the '940 patent. The claims are identical except that claims 106, 109, 112, 115, 118 and 121 recite "crystallize" instead of "polycrystallize" and "crystalline" instead of "polycrystalline."

Having complied with the requirements of 37 CFR § 1.607, the Applicants respectfully request that the Examiner proceed in accordance with 37 CFR § 1.607(b). The Applicants respectfully submit that the examination of the present application, including the appeal before the Board, be conducted with special dispatch. The Applicants request that the Examiner indicate that there is interfering subject matter claimed in the present application, that the '940 patent is patentable to the Applicants, that the '940 patent is subject to a judgment in an interference, and that an interference be declared.

Since the present application has an earlier effective filing date than the '940 patent (noted in detail above), the Applicants respectfully request that they be designated the senior party in a declaration of the interference.

Should the Examiner believe that anything further would be desirable to place this application in better condition for allowance or interference, the Examiner is invited to contact the Applicants' undersigned attorney at the telephone number listed below.

Respectfully submitted,


Eric J. Robinson
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Receipt is acknowledged on: June 17, 1999

In re the New Divisional Application of: Shunpei YAMAZAKI et al.
Based on Serial No. 08/938,310 (0756-1727) Filed: September 26, 1997
For: SEMICONDUCTOR DEVICE AND FABRICATION METHOD THEREOF

Utility Patent Application Transmittal
Fee Transmittal (duplicate)

Copy of specification, abstract and new claims
Copy of Declaration and Power of Attorney as originally filed
Eight (8) sheets of formal drawings
Preliminary Amendment (2 pages)
Information Disclosure Statement w/PTO Form-1449
Notice of Change of Address
Check No. 67418 in the amount of \$1,972.00
(\$760 Filing Fee, \$666 Add'l Clms Fee, \$546 Add'l Indep Clms Fee)



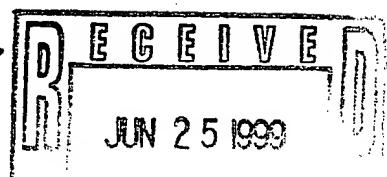
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Sixbey, Friedman,
Leedom & Ferguson





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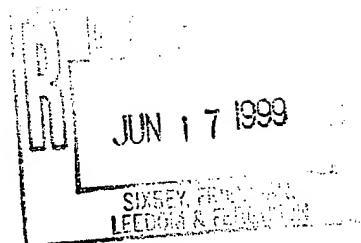
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